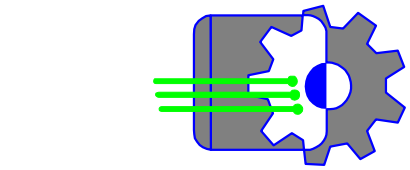
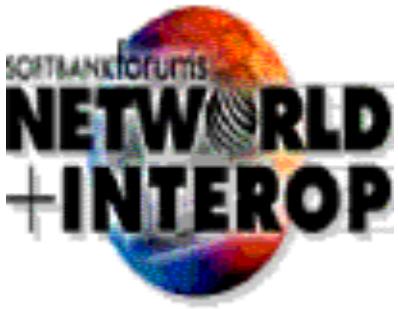


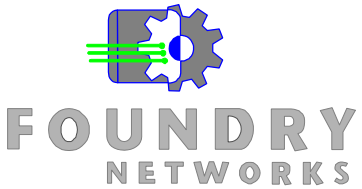




# Real Routing at Gigabit Speeds

Earl Ferguson - CTO - Foundry Networks

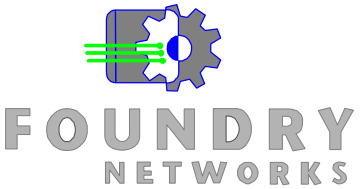
Presented at

Networld+Interop 97 - Atlanta



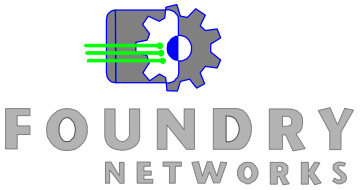

# What is “Real” Routing


- Forwarding by Destination IP Address
- Proper interpretation and updating of packet headers
- RIP, RIP2, OSPF Topology Updates for the Intranet + BGP4 for the Internet
- DVMRP and PIM for Multicast Control and Routing




# Real Routing Needs


- Internet OR Intranet
  - Both Require “Real” Routing
- Internet
  - Requires Very Large Route Tables
    - » Host Based Routing is Problematic
  - Intermediate Speeds
- Intranet
  - Limited Size Route Tables
    - » Can Use Host Based Routing
  - Needs Absolute Speed



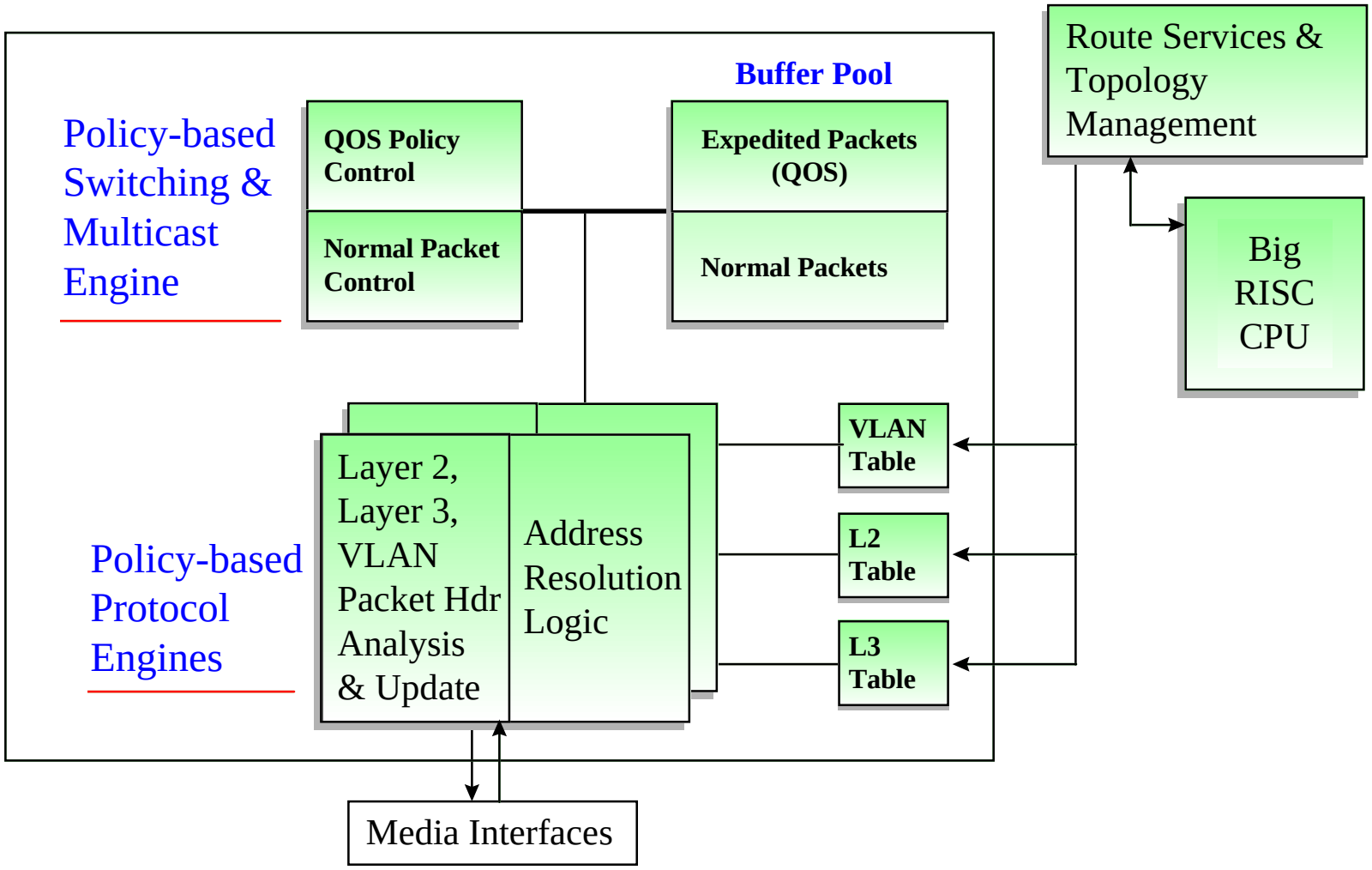

# The Foundry Approach

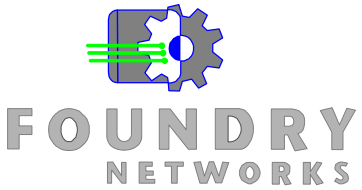

- Route Cache
  - IP and IPX
- ASIC IP and IPX Forwarding
  - Header Verification
  - Route Lookup
  - MAC Address Substitution
  - TTL Decrement and Checksum Update
- Processor Based Management
  - Exception Routing
  - Error handling
  - OSPF, RIP, DVMRP, PIM, ...

# Host Route Cache

- CAM Lookup
  - MAC Addresses
  - L3 Addresses
- SRAM Tables
  - Forwarding Information
    - » L2 - Port(s), VLANs, Priority
    - » L3 - Next hop MAC Address, Port(s), Priority
  - Aging

# Switching Router Architecture






# ASIC IP Forwarding

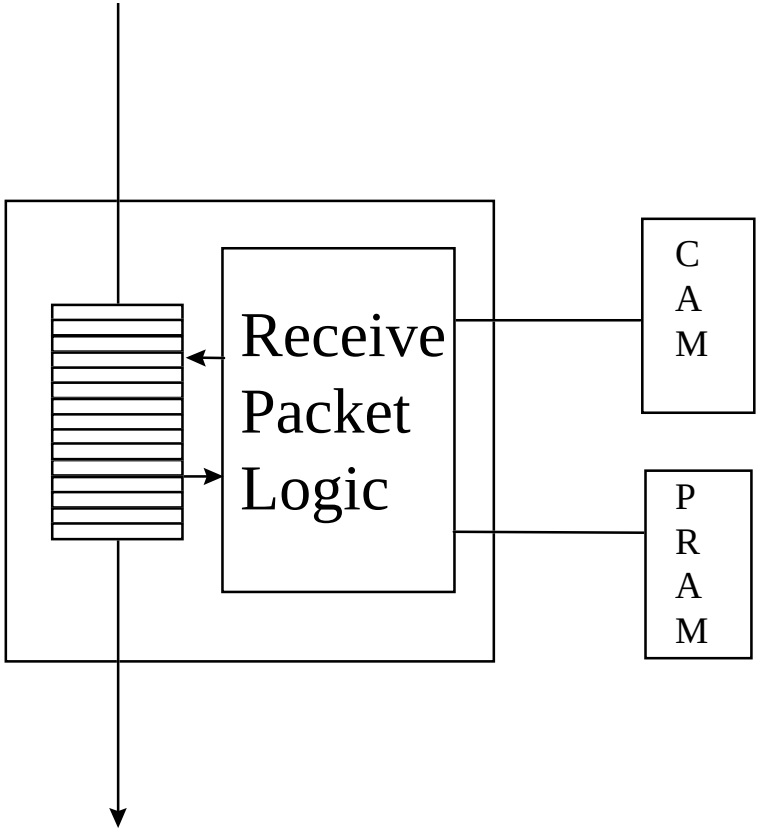

- MAC DA to this Router
- IPv4 & IP Header Len = 5
- TTL > 1
- Destination IP Lookup
- Substitute MAC Address
- Forward to Correct Output Port
- Decrement TTL
- Update Checksum

# ASIC IPX Forwarding

- MAC DA to this Router
- Transport Control < 16
- Destination IPX Network Lookup
- Substitute MAC Address
- Forward to Correct Output Port
- Increment Transport Control

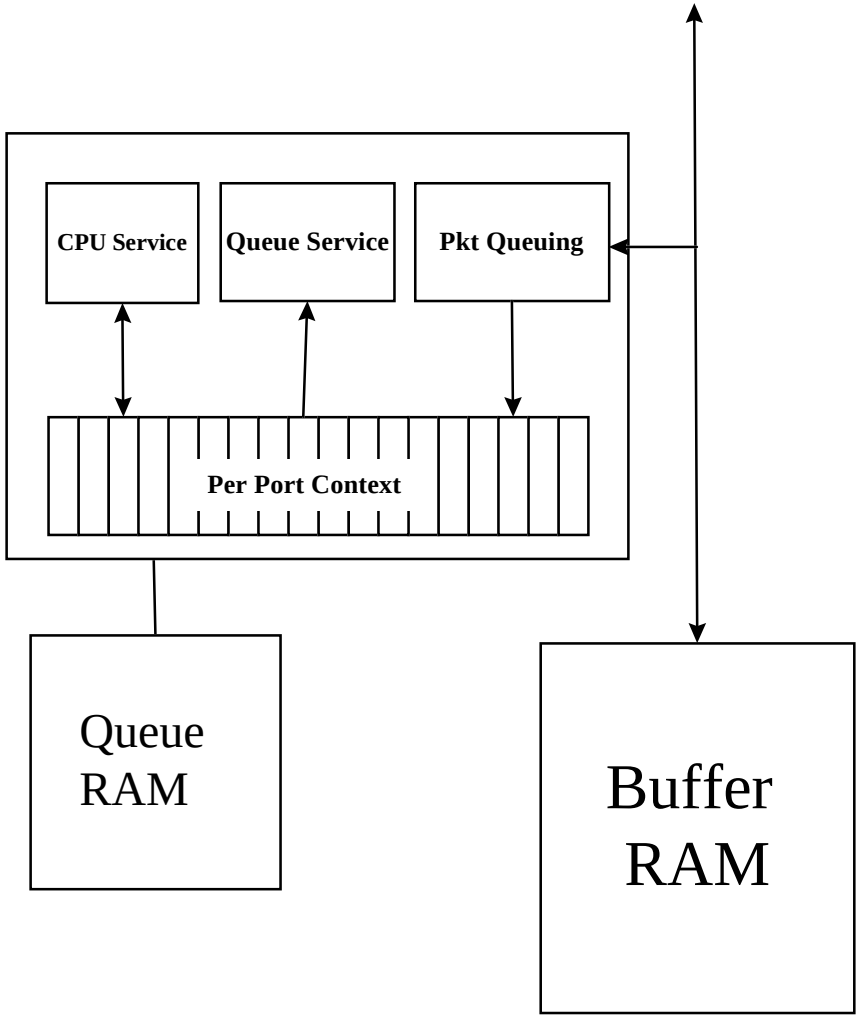
# Receive Packet Processing - the Hardware

- CAM DA and SA Lookups and Aging
- CAM L3 Lookup and Aging
- Priority and Forwarding Control from PRAM
- VLAN Tag Stripping & Packet Stamping
- L3 Packet Modification from PRAM
  - DA Substitution



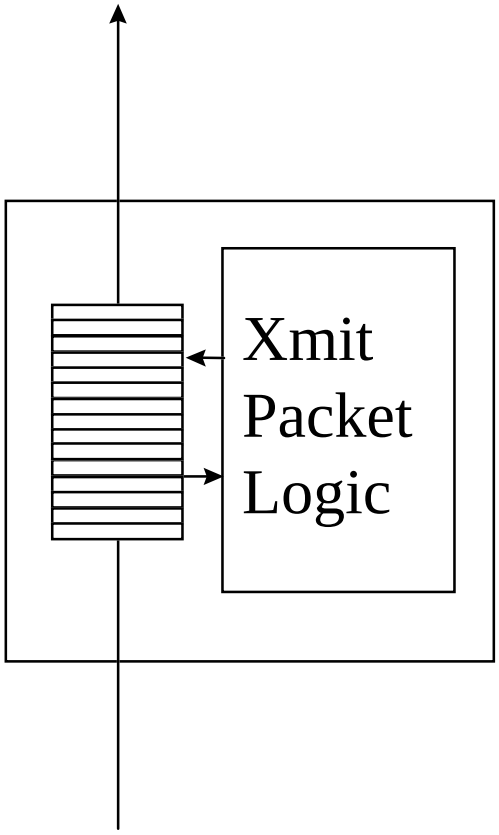
# Switch Processor

- Buffer Control and Management
- Priority Queuing to Tx Port
- Multicast Queuing to Multiple Ports
- Traffic Flow Management
- CPU Queuing and Buffer Access



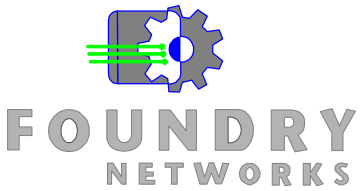
# Transmit Packet Processing

- Per Port FIFOs
- VLAN Tagging
- SA Substitution
- L3 TTL and Checksum Updates
-



# Performance

- 1.5 M Packets per Second per Port
  - Limited by Port Bandwidth
- Processor Routing at ~500Kpps
- Full Wirespeed on ports up to Gigabit Ethernet Speeds




# Summary


- Intranet Routing at Wirespeed is Achieved Today
- Internet Routing has Different Challenges in the Route Table Sizes
- For the Immediate Future, there will continue to be separate solutions for Intranets and the Internet