Processing packets in packet switches

CS343
May 7th 2003

Nick McKeown
Professor of Electrical Engineering
and Computer Science, Stanford University
nickm@stanford.edu
www.stanford.edu/~nickm

Contents

1. What processing is done where?
2. What does a packet switch look like?
   - Examples of packet switches
   - What does a packet switch do?
   - Typical packet switch architecture
   - Evolution of high performance packet switch architecture
3. Trends and consequences
4. Technology options for processing packets
   - General purpose CPU
   - Network processors
   - FPGA
   - ASIC
5. My 2c
The Network Layer View of the Internet

Hierarchical arrangement

* A crude approximation

End hosts

Routers

Core Routers

Edge Routers

Core routers: Maximum capacity, minimum function
Typically: 16 ports of 10Gb/s, Capacity 160Gb/s, 200Mpps, Price $1M

Edge routers: Medium capacity, maximum flexibility and function
Typically: 16 ports of 2.5Gb/s, Capacity 20-30 Gb/s, 10-20Mpps, Price $200k
Hierarchical arrangement

End hosts (1000s per mux)
Access multiplexer
Edge Routers
Core Routers
Point of Presence (POP)

POP: Point of Presence. Richly interconnected by mesh of long-haul links.
Typically: 40 POPs per national network operator; 10-40 core routers per POP.

Autonomous Systems

POP
POP
POP
POP
Worldcom
"peering points"

POP
POP
POP
Sprint

POP
POP
POP
AT&T

POP
POP
POP
Global Crossing
How we connect
Corporate/campus Environment

Building-wide router
e.g. gates-emc.stanford.edu
Typically 16 ports of 16 Mb/s Ethernet

Ethereal

Typically 100 ports of 100Mb/s Ethernet

Campus or company-wide router
e.g. border-emc.stanford.edu
Typically mixture of 2.5Gb/s "OC48" and 6Gb/s Ethernet

POP

10Gb/s "OC192"

How we connect
Home modem/DSL environment

Telephone switch with DSL line interface at your local Central Office

Point of Presence (POP)

DSL Router/NAT
Typically: 10/100Mb/s

1/8
Outline

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What a High Performance Router Looks Like

- **Cisco GSR 12416**
  - 19"
  - 6ft
  - Capacity: 160Gb/s
  - Power: 4.2kW

- **Juniper M160**
  - 19"
  - 3ft
  - Capacity: 80Gb/s
  - Power: 2.6kW
Other packet switches

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The IP Datagram

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>vers</td>
<td>Variable</td>
</tr>
<tr>
<td>HLen</td>
<td>Header Length</td>
</tr>
<tr>
<td>TOS</td>
<td>Type of Service</td>
</tr>
<tr>
<td>Total Length</td>
<td>Total Length</td>
</tr>
<tr>
<td>ID</td>
<td>Identification Sequence</td>
</tr>
<tr>
<td>Flags</td>
<td>Flags</td>
</tr>
<tr>
<td>FRAG Offset</td>
<td>Fragment Offset</td>
</tr>
<tr>
<td>TTL</td>
<td>Time to Live</td>
</tr>
<tr>
<td>Protocol</td>
<td>Protocol Type</td>
</tr>
<tr>
<td>checksum</td>
<td>Checksum</td>
</tr>
<tr>
<td>SRC IP Address</td>
<td>Source IP Address</td>
</tr>
<tr>
<td>DST IP Address</td>
<td>Destination IP Address</td>
</tr>
<tr>
<td>OPTIONS</td>
<td>Options</td>
</tr>
<tr>
<td>PAD</td>
<td>Padding</td>
</tr>
</tbody>
</table>

Forwarding in an IP Router

1. Lookup packet DA in forwarding table.
   - If known, forward to correct port.
   - If unknown, drop packet.
2. Decrement TTL, update header checksum.
3. Forward packet to outgoing interface.
4. Transmit packet onto link.
**Ethernet Frame Format**

<table>
<thead>
<tr>
<th>Bytes</th>
<th>7</th>
<th>1</th>
<th>6</th>
<th>6</th>
<th>2</th>
<th>0-1500</th>
<th>0-46</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preamble</td>
<td>SFD</td>
<td>DA</td>
<td>SA</td>
<td>Type</td>
<td>Data</td>
<td>Pad</td>
<td>CRC</td>
<td></td>
</tr>
</tbody>
</table>

1. Preamble: trains clock-recovery circuits
2. Start of Frame Delimiter: indicates start of frame
3. Destination Address: 48-bit globally unique address assigned by manufacturer;
   1b: unicast/multicast
   1b: local/global address
4. Type: Indicates protocol of encapsulated data (e.g. IP = 0x0800)
5. Pad: Zeros used to ensure minimum frame length
6. Cyclic Redundancy Check: check sequence to detect bit errors.

**Encapsulation**

![Encapsulation Diagram](image)

<table>
<thead>
<tr>
<th>IP Header</th>
<th>IP Data</th>
</tr>
</thead>
</table>

| Preamble | SFD | DA | SA | Type | IP | Data | Pad | CRC |

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16
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Generic Router Architecture
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First Generation Routers

Typically <0.5Gb/s aggregate capacity

Second Generation Routers

Typically <5Gb/s aggregate capacity
Third Generation Routers

Switched Backplane

Typically <50Gb/s aggregate capacity

Fourth Generation Routers

Switch Core

Linecards

Optical links

100s of metres

160Gb/s - 20Tb/s routers in development
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Trends in Technology, Routers & Traffic

- Line Capacity: 2x / 7 months
- User Traffic: 2x / 10 months
- Router Capacity: 2.2x / 18 months
- Moore’s Law: 2x / 18 months
- DRAM Random Access Time: 1.1x / 18 months
Trends and Consequences

1. CPU Instructions per minimum length packet

2. Disparity between traffic and router growth

Consequences:
1. Packet processing is getting harder, and eventually network processors will be used less for high performance routers.
2. (Much) bigger routers will be developed.

Trends and Consequences (2)

3. Power consumption will exceed POP limits

4. Disparity between line-rate and memory access time

Consequences:
3. Multi-rack routers will spread power over multiple racks.
4. It will get harder to build packet buffers for linecards.
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Technology Options

- **General purpose processor**
  - MIPS
  - PowerPC
  - Intel

- **Network processor**
  - Intel IXA and IXP processors
  - IBM Rainier
  - Control plane processors: SiByte (Broadcom), QED (PMC-Sierra).

- **FPGA**
- **ASIC**
Network Processors
Load-balancing

Incoming packets dispatched to:
1. Idle processor, or
2. Processor dedicated to packets in this flow (to prevent missequencing).
3. Processor for processing needed by packet, e.g. security, transcoding, application-level processing.

Network Processors
Pipelining

Processing broken down into (hopefully balanced) steps. Each processor performs one step of processing.
Network Processors

Pros
- Flexibility: Protocols change, features are added.
- Reduced development time: In principle, should be quicker to develop software than design a custom chip.
- Reduces time-to-market, development costs, ...

Cons
- Less efficient: slower than custom chip, more power.
- Usually designed using standard processors cores, not optimized for stream processing.
- Generally about 10x slower than general purpose CPU.
- Unusual development environments: hard to program.
- Often hard to partition functions over processors.

General Observations

❖ Up until about 1998,
  - Low-end packet switches used general purpose processors.
  - Mid-range packet switches used FPGAs for datapath, general purpose processors for control plane.
  - High-end packet switches used ASICs for datapath, general purpose processors for control plane.

❖ More recently,
  - 3rd party network processors now used in many low- and mid-range datapaths.
  - Home-grown network processors used in mid- and high-end.
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My 2c on network processors

- Is it clear that multiple small parallel processors are needed?
- When are 10 processors at speed 1 better than 1 processor at speed 10?
- Network processors make sense if:
  - Application is parallelizable into multiple threads/contexts,
  - Uniprocessor performance is limited by load-latency.
- If general purpose processors evolve anyway to:
  - Contain multiple processors per chip,
  - Support hardware multi-threading,
- ...then perhaps they are better suited because:
  - Greater development effort means faster general purpose processors,
  - Existing well-known development environments.
**My 2c on network processors**

The nail:

![Diagram of network processors]

Characteristics:
1. Stream processing.
2. Multiple flows.
3. Most processing on header, not data.
4. Two sets of data: packets, context.
5. Pockets have no temporal locality, and special spatial locality.
6. Context has temporal and spatial locality.

The hammer:

![Diagram of data cache and context]

Characteristics:
- Shared input bus.
- Optimized for data with spatial and temporal locality.
- Especially optimized for register accesses.

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**A network uniprocessor**

![Diagram of network uniprocessor]

Add hardware support for multiple threads/contexts.