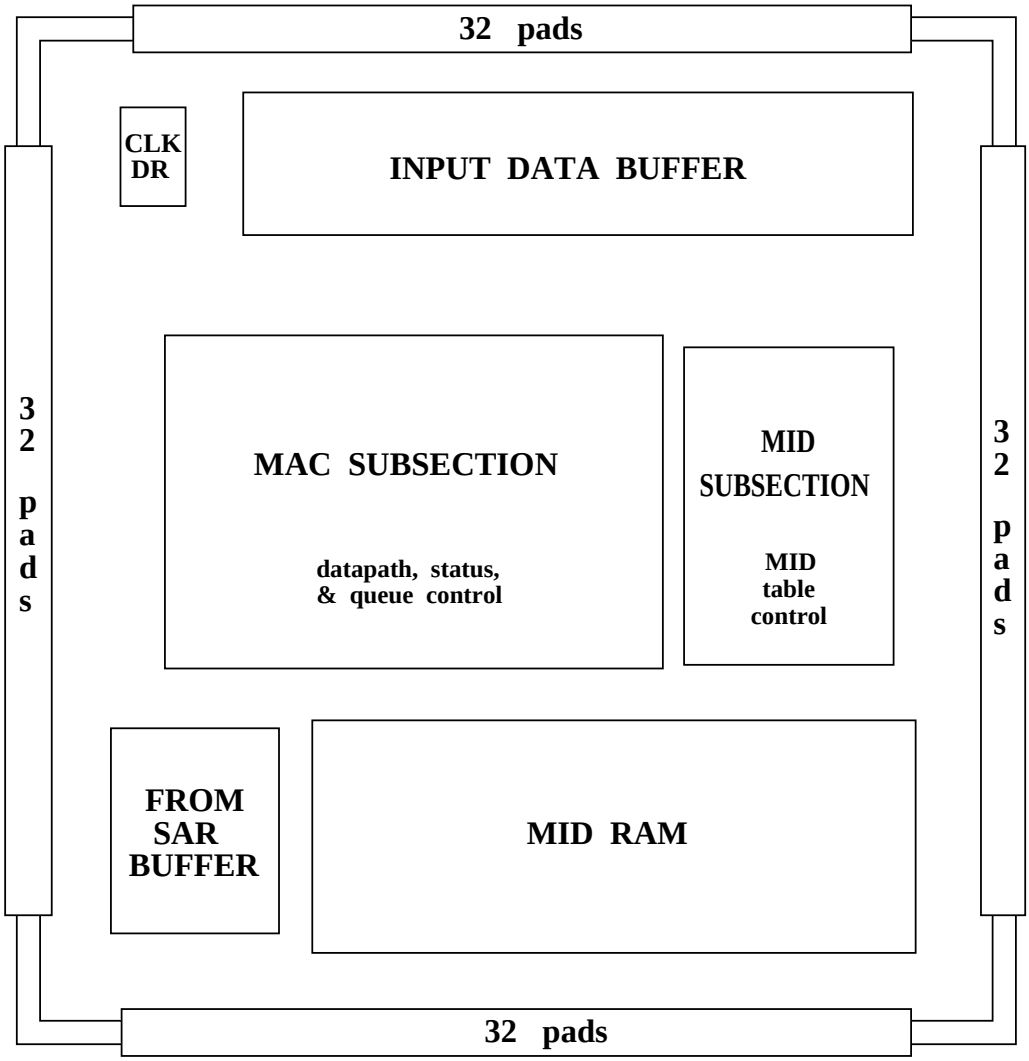
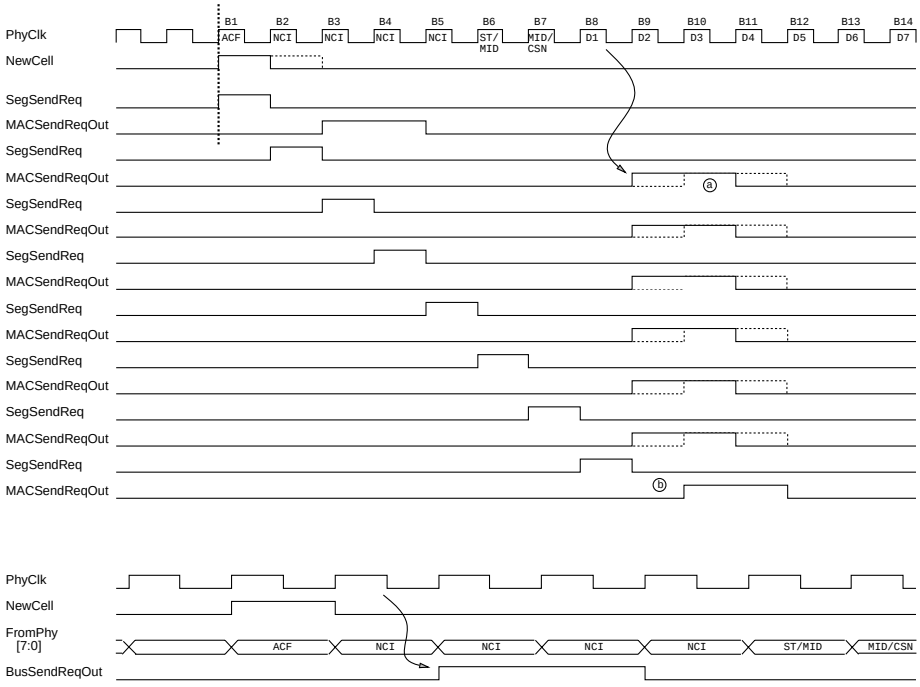
8 FLOORPLAN


32 pads
CLK DR
INPUT DATA BUFFER
32 pads
MAC SUBSECTION
datapath, status, & queue control
MID SUBSECTION
MID table control
32 pads
FROM SAR BUFFER
MID RAM
32 pads

7.4 DQDB QUEUE HANDSHAKING



MACSendReqIn and BusSendReqIn can be asserted at any time. Both should be asserted for two cycles.

ⓐ Request Counter = 0 Request Counter <> 0

ⓑ This timing relationship between SegSendReq and MACSendReqOut is maintained EXCEPT immediately after NewCell as shown above.

BXX - byte number XX from NewCell (ACF is byte 1).
DXX - data byte number XX (data byte 1 is immediately after the header).

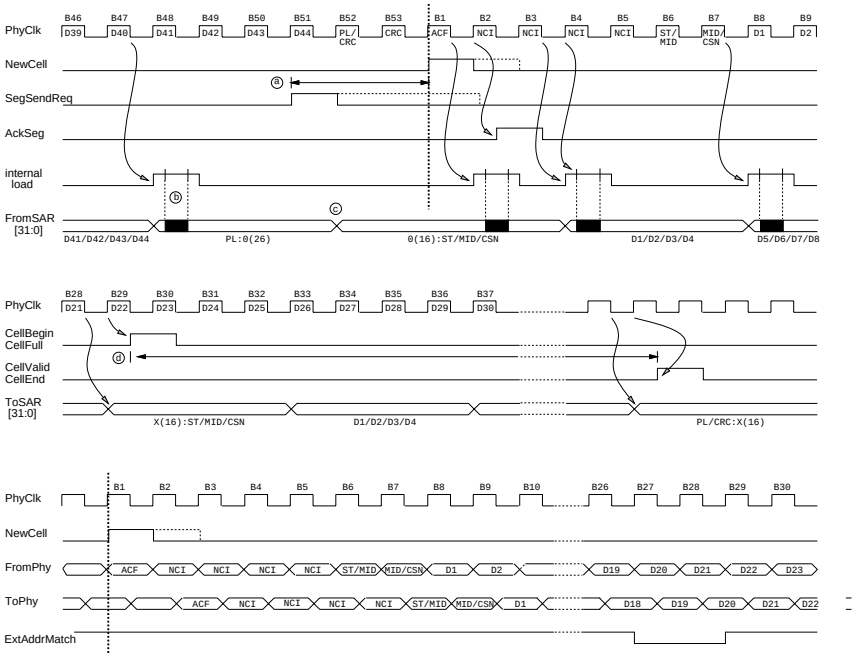
PhyClk edge responsible for output transtion.

Beginning of cell

7.3 PHYSICAL AND SAR INTERFACES (STS3)

PHYSICAL AND SAR INTERFACE TIMING

(STS3)



ⓐ SegSendReq can be asserted at any time. However, for a send to occur in the cell immediately following, it must be asserted at least three cycles before NewCell.

ⓑ The solid black area is the time during which the data inputs are sampled.

ⓒ It is recommended that the first two bytes from Segmentation be applied and held with assertion of SegSendReq, since the time between SegSendReq and latching of the first two bytes is not guaranteed.

ⓓ There are always exactly 48 cycles between the rising edge of CellBegin (CellFull) and the rising edge of CellEnd (CellValid).

BXX - byte number XX from NewCell (ACF is byte 1).

DXX - data byte number XX (data byte 1 is immediately after the header).

PhyClk edge responsible for output transtion.

Maximum pulse width (single cycle recommended)

Beginning of cell

(V2)

7.2 OUTPUT

OUTPUT TIMING

	TPLH	TPHL	SETUP	WIDTH	FIG	POSITION
			(STS3)	(cycles)		cell byte #
CellBegin	25	22	26	1	1	29
CellFull	25	22	26	1	1	29
CellValid	25	22	26	1	1	CellBegin + 48
CellEnd	25	22	26	1	1	CellBegin + 48
ToSAR[31:0]	23*	21*	28	---	2	29**
AckSeg	24	21	27	1	1	2
ToPhy[7:0]			TO BE MEASURED			
MACSendReqOut	22	19	29	2	2	---
BusSendReqOut	22	19	29	2	2	---
TestPoint	24	21	27	2	1	---
ScanOut	23	20	28	2	1	---

* Maximum.

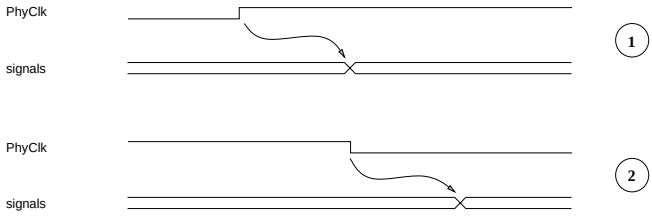
** The first word is delivered at byte 29. The remaining 12 words follow at 4 cycle intervals.

--- Does not apply.

All time values are in nanoseconds.

SETUP is the approximate maximum time between an output change of state and the next rising edge of PhyClk at STS3 (51.44ns period). This value is not guaranteed.

Approximate rise time is 4.5ns. Approximate fall time is 3.0ns.



Version 2 timing requires electrical verification after fab.
The numbers above are approximate expected values. **(V2)**

7 TIMING

7.1 INPUT

INPUT TIMING

PhyClk: 50% duty cycle nominal. DS3 - 205.76ns period. STS3 - 51.44ns period.

	SETUP				HOLD				FIGURE	POSITION
	min	units	max	units	min	rec*	max	units		cell byte #
NewCell	5	ns	3/4	cycle	1	1	2	cycle(s)	1	1
ExtAddrMatch	0	ns	1/4	cycle	2	**	---	cycle(s)	3/	27
FromPhy[7:0]	0	ns	1/4	cycle	1	---	---	cycle(s)	3	see p.
SegSendReq	5	ns	3/4	cycle	1	1	4	cycle(s)	1	---
fromSAR[31:0]	0	ns	1/4	cycle	1	---	---	cycle(s)	3	see p.
MACSendReqIn	0	ns	3/4	cycle	1	2	3	cycle(s)	2	---
BusSendReqin	0	ns	3/4	cycle	1	2	3	cycle(s)	2	---
Init	0	ns	---		1	2	***	cycle(s)	---	---
Resetn	0	ns	---		1	2	***	cycle(s)	---	---
Mode	0	ns	1/4	cycle	1	---	---	cycle(s)	3	---
ScanIn	0	ns	1/4	cycle	1	---	---	cycle(s)	3	---
ShiftConst	0	ns	1/4	cycle	1	---	---	cycle(s)	3	---
Const	0	ns	1/4	cycle	1	---	---	cycle(s)	3	---

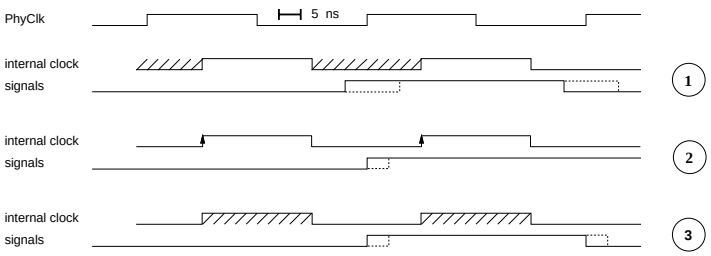
* recommended

** ExtAddrMatch can be held until evaluation is complete for the next cell.

*** indefinitely

--- Does not apply (hold) or at any time (position).

All setup and hold values relative to the rising edge of PhyClk.
Numbers in the table above are valid for both DS3 and STS3. The diagrams below are specific to STS3.



-- evaluation period (level sensitive latch)

-- evaluation edge (edge sensitive flip-flop)

-- signal internal delay

Version 2 timing requires electrical verification after fab. (V2)
The numbers above are approximate expected values.

6.3 PACKAGE LAYOUT

	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
1	32	29	26	24	23	20	19	14	13	10	7	5	2	131	1
2	35	33	30	27	25	21	18	15	12	9	6	3	132	128	2
3	38	36	34	31	28	22	17	16	11	8	4	1	129	125	3
4	40	39	37									130	126	123	4
5	43	42	41									127	124	122	5
6	46	45	44									121	120	119	6
7	47	48	49									116	117	118	7
8	52	51	50									115	114	113	8
9	53	54	55									110	111	112	9
10	56	58	61									107	108	109	10
11	57	60	64									103	105	106	11
12	59	63	67	70	74	77	82	83	88	94	97	100	102	104	12
13	62	66	69	72	75	78	81	84	87	91	93	96	99	101	13
14	65	68	71	73	76	79	80	85	86	89	90	92	95	98	14
	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

FromSAR[27]	67
GND	68
FromSAR[26]	69
FromSAR[25]	70
FromSAR[24]	71
FromSAR[23]	72
Vdd	73
FromSAR[22]	74
FromSAR[21]	75
FromSAR[20]	76
FromSAR[19]	77
GND	78
FromSAR[18]	79
FromSAR[17]	80
FromSAR[16]	81
FromSAR[15]	82
Vdd	83
FromSAR[14]	84
FromSAR[13]	85
FromSAR[12]	86
FromSAR[11]	87
GND	88
FromSAR[10]	89
FromSAR[9]	90
FromSAR[8]	91
FromSAR[7]	92
Vdd	93
FromSAR[6]	94
FromSAR[5]	95
FromSAR[4]	96
FromSAR[3]	97
GND	98
FromSAR[2]	99
FromSAR[1]	100
Vdd	101
FromSAR[0]	102
AckSeg	103
SegSendReq	104
TP1	105
GND	106
ScanOut	107
TP2	108
ScanIn	109
Mode	110
Vdd	111
TP3	112
TP4	113
Init	114
Reset	115
GND	116
Const	117
ShiftConst	118
CellValid	119
CellEnd	120
Vdd	121
CellFull	122
CellBegin	123
ToSAR[0]	124
ToSAR[1]	125
GND	126
ToSAR[2]	127
ToSAR[3]	128
ToSAR[4]	129
ToSAR[5]	130
Vdd	131
ToSAR[6]	132

6.2 by POSITION

ToSAR[7]	1	FromPhy[0]	34
GND	2	Vdd	35
ToSAR[8]	3	FromPhy[1]	36
ToSAR[9]	4	FromPhy[2]	37
ToSAR[10]	5	FromPhy[3]	38
ToSAR[11]	6	FromPhy[4]	39
Vdd	7	GND	40
ToSAR[12]	8	FromPhy[5]	41
ToSAR[13]	9	FromPhy[6]	42
ToSAR[14]	10	FromPhy[7]	43
ToSAR[15]	11	NewCell	44
GND	12	Vdd	45
ToSAR[16]	13	MACSendReqIn	46
ToSAR[17]	14	BusSendReqOut	47
ToSAR[18]	15	BusSendReqIn	48
ToSAR[19]	16	MACSendReqOut	49
Vdd	17	GND	50
ToSAR[20]	18	ExtAddrMatch	51
ToSAR[21]	19	ToPhy[0]	52
ToSAR[22]	20	ToPhy[1]	53
ToSAR[23]	21	ToPhy[2]	54
GND	22	Vdd	55
ToSAR[24]	23	ToPhy[3]	56
ToSAR[25]	24	ToPhy[4]	57
ToSAR[26]	25	ToPhy[5]	58
ToSAR[27]	26	ToPhy[6]	59
Vdd	27	GND	60
ToSAR[28]	28	ToPhy[7]	61
ToSAR[29]	29	FromSAR[31]	62
ToSAR[30]	30	FromSAR[30]	63
ToSAR[31]	31	FromSAR[29]	64
GND	32	Vdd	65
PhyClk	33	FromSAR[28]	66

6 PINOUT

6.1 by FUNCTION

CellBegin	123		
CellFull	122		
CellEnd	120	SegSendReq	104
CellValid	119	AckSeg	103

FromSAR[31]	62	ToSAR[31]	31
FromSAR[30]	63	ToSAR[30]	30
FromSAR[29]	64	ToSAR[29]	29
FromSAR[28]	66	ToSAR[28]	28
FromSAR[27]	67	ToSAR[27]	26
FromSAR[26]	69	ToSAR[26]	25
FromSAR[25]	70	ToSAR[25]	24
FromSAR[24]	71	ToSAR[24]	23
FromSAR[23]	72	ToSAR[23]	21
FromSAR[22]	74	ToSAR[22]	20
FromSAR[21]	75	ToSAR[21]	19
FromSAR[20]	76	ToSAR[20]	18
FromSAR[19]	77	ToSAR[19]	16
FromSAR[18]	79	ToSAR[18]	15
FromSAR[17]	80	ToSAR[17]	14
FromSAR[16]	81	ToSAR[16]	13
FromSAR[15]	82	ToSAR[15]	11
FromSAR[14]	84	ToSAR[14]	10
FromSAR[13]	85	ToSAR[13]	9
FromSAR[12]	86	ToSAR[12]	8
FromSAR[11]	87	ToSAR[11]	6
FromSAR[10]	89	ToSAR[10]	5
FromSAR[9]	90	ToSAR[9]	4
FromSAR[8]	91	ToSAR[8]	3
FromSAR[7]	92	ToSAR[7]	1
FromSAR[6]	94	ToSAR[6]	132
FromSAR[5]	95	ToSAR[5]	130
FromSAR[4]	96	ToSAR[4]	129
FromSAR[3]	97	ToSAR[3]	128
FromSAR[2]	99	ToSAR[2]	127
FromSAR[1]	100	ToSAR[1]	125
FromSAR[0]	102	ToSAR[0]	124

TP1

TP1 monitors the status of the MID_table_valid interface signal between the MID subsection and the MAC subsection. MID_table_valid (active high) indicates when the time stamp for a given MID is valid.

TP2

When in Scan mode, TP2 monitors an intermediate location in the scan path, between the MID Table Control circuitry and the rest of the MAC state.

When in Normal mode, TP2 can be used as a status flag that is active (low) when a valid BOM or SSM is received and the MID table entry is valid before the time stamp is applied.

TP3

TP3 monitors the status of the enableWrite signal in the MID subsection. This signal is active when a time stamp is written to the MID table.

TP4

TP4 monitors the ready_to_send signal in the MAC subsection. This signal is active (low) when the following condition is true: send request queued AND count down counter equals zero AND bandwidth balancing counter does not equal zero. When ready_to_send is asserted, data will be transmitted to the physical layer when the next empty cell (busy bit = 0) arrives.

AUXILIARY PINS

ExtAddrMatch (Input, active low)

ExtAddrMatch is asserted by an external address comparator when the destination address in a BCM cell matches one of a set of addresses for the local node.

ExtAddrMatch must be asserted **before or at the same time as the 27th byte of the cell**, and held for two cycles.

Init (Input, active high)

Init resets the state of the MAC and begins a MID table initialization sequence. The MID table initialization takes approximately 16,000 cycles. All entries of the MID table are set to **invalid**.

Reset (Input, active low)

Reset puts the MAC in a known starting state, ready to process data.

Const (Serial Data Input)

Const is a serial data input used during the **Counter Constant Loading** process. The first eight bits program the Bandwidth Balancing Counter, and the second eight bits set the period of the MID table time-out algorithm.

ShiftConst (Input, active high)

ShiftConst controls shifting of the serial data stream at Const. When high, data is shifted with CLOCK, when low, there is no change.

Mode (Input, active high)

Mode switches the scan path between Scan mode and Normal mode. In Scan mode, MAC state can be serially loaded at ScanIn and serially read at ScanOut. In normal mode (Mode = 0), the scan path is disabled.

ScanIn (Serial Data Input)

ScanIn is the MAC state scan path input.

ScanOut (Serial Data Output)

ScanOut is the MAC state scan path output.

latched during the positive half cycle just prior to assertion of AckSeg. New data is required at FromSAR[31:0] by the second rising edge following assertion of AckSeg.

It is recommended that the initial half_word of each DQDB payload be held stable at FromSAR[15:0] until AckSeg is asserted, since the time between SegSendReq and AckSeg is not guaranteed.

MAC INTERFACE

MACSendReqIn (Input, active high)

MACSendReqIn is asserted by the MAC on the opposite bus when it has data to transmit. MACSendReqIn is connected to MACSendReqOut of the corresponding MAC (on the opposite bus).

MACSendReqOut (Output, active high)

MACSendReqOut is asserted shortly after SegSendReq is asserted. The corresponding MAC (on the opposite bus) registers the request in a local counter, and will set the Request bit of a cell passing on the opposite bus if that Request bit is cleared. The local counter is decremented when a Request bit is set. MACSendReqOut is connected to MACSendReqIn of the corresponding MAC.

BusSendReqIn (Input, active high)

BusSendReqIn is asserted by the MAC on the opposite bus when the request bit of a cell passing on that bus is set. The MAC registers the request by incrementing its Request Counter by one. BusSendReqIn is connected to BusSendReqOut of the corresponding MAC.

BusSendReqOut (Output, active high)

BusSendReqOut is asserted when the Request bit of a cell passing on the bus is set. The Request bit indicates that a downstream node on the opposite bus has data to transmit. This action queues the request in the corresponding MAC.

BusSendReqOut is connected to BusSendReqIn of the corresponding MAC.

CellFull (Output, active high)

CellFull is asserted at the same time as CellBegin if the following conditions are met:

- The cell Destination Address matches the node address, or the MID table entry is valid.
- The NCI is valid.
- The busy bit is set.

CellValid (Output, active high)

CellValid is asserted at the same time as CellEnd if the following conditions are met:

- The payload length is correct
- The CRC is correct
- The CellFull signal was asserted at the start of the current cell.

CellEnd (Output, active high)

CellEnd is asserted on the falling edge of CLOCK one-half cycle after ToSAR[31:0] changes value. It signals that ToSAR[31:16] represent the last two bytes of the cell payload. ToSAR[15:0] is invalid for the last word.

SegSendReq (Input, active high)

SegSendReq is asserted by the Segmentation unit when data is ready to be transmitted. When the MAC detects SegSendReq, the value in the Request Counter is loaded into the Count Down Counter, MACSendReq is asserted, and the request is queued for sending when the proper DQDB queue conditions are met.

Once a send request has been made, SegSendReq must not be asserted again until AckSeq is received by the Segmentation unit.

For the first 32 bit word in each DQDB payload, the MAC reads only the low half-word (FromSAR[15:0]), and ignores FromSAR[31:16].

AckSeg (Output, active high)

AckSeg is asserted on the falling edge of CLOCK when queue conditions have been met for transmission of cells to the Physical Layer. FromSAR[15:0] is

5 PIN DESCRIPTIONS

PHYSICAL LAYER INTERFACE

FromPhy[7:0] (Inputs)

8 bits of data from the Physical Layer. Data is received at the rate of 20MHz, and is read while the CLOCK is high. The first byte of each cell should arrive coincident with assertion of NewCell (also from Physical Layer).

ToPhy[7:0] (Outputs)

8 bits of data to the Physical Layer. Data is either a retransmission of cells received by the local node or transmission of local data in place of an empty cell. ToPhy[7:0] is valid within a window surrounding the rising edge of the CLOCK.

SAR INTERFACE

FromSAR[31:0] (Inputs)

32 bits of data from the Segmentation unit of the SAR board. Data is received at the rate of 5MHz (internally generated clock), and is read while CLOCK is high.

ToSAR[31:0] (Outputs)

32 bits of data to the Reassembly unit of the SAR board. Data changes value after every fourth rising edge of the CLOCK. ToSAR[31:0] is synchronized to the Reassembly unit with the CellBegin and CellEnd signals.

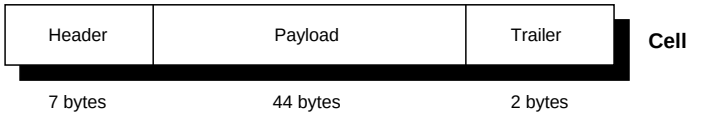
NewCell (Input, active high)

NewCell is used to indicate the arrival of a new cell from the Physical Layer. NewCell should be asserted on the rising edge of CLOCK coincident with arrival of the first byte of the cell.

CellBegin (Output, active high)

CellBegin is asserted on the falling edge of CLOCK one-half cycle after ToSAR[31:0] is stable. It indicates that the values on ToSAR[15:0] represent the first two bytes of the cell payload. ToSAR[31:16] is invalid for the first word.

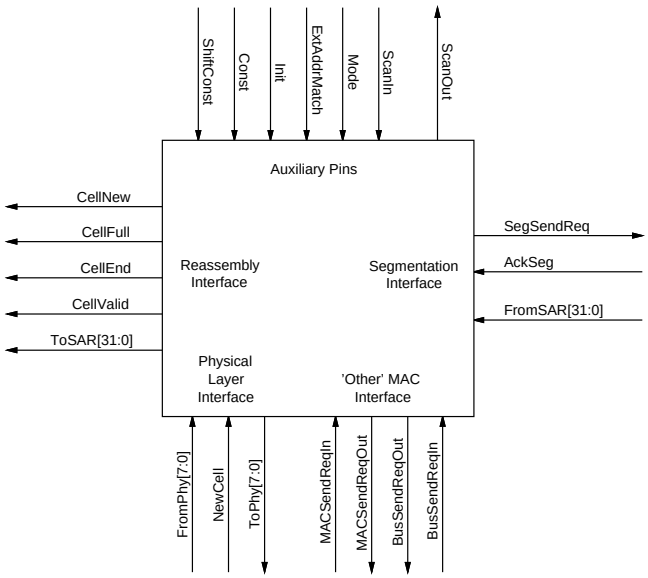
3 CELL STRUCTURE



ACF (Access Control field) - 8 bits
NCI (Network Control Information) - 32 bits
ST (Slot Type) - 2 bits
MID (Message Identifier) - 10 bits
SN (Sequence Number) - 4 bits

PLL (Payload Length) - 6 bits
CRC (Payload CRC) - 10 bits

4 LOGIC SYMBOL



- Managing the local DQDB queue

  The MAC fully implements the DQDB Queueing protocol.

  The Request Counter registers outstanding requests for bandwidth. These requests are made by other MACs on the same bus.

  The Count Down Counter is loaded with the contents of the Request Counter when the MAC receives a SegSendReq from the Segmentation unit, and decremented each time an empty cell passes through the Physical Layer. Sending is allowed when the Count Down Counter reaches zero.

  The Bandwidth Balancing Counter limits the number of consecutive cells that can be transmitted.

  DQDB queue management requires communication between the two MACs in a node. When the MAC on bus A (MACA) has data to transmit, it sends a request for bandwidth to its companion MAC (MACB). MACB then sets the Request bit of a cell on bus B, if that bit is clear. When MACs on bus B *downstream* from MACB detect the set Request bit, they signal the bus A MAC in their node to register the request in the bus A Request Counter. In this way, MACs on bus A *upstream* from the requesting MACA will allow empty cells to pass to satisfy the bandwidth requirement.

  This procedure is symmetric for bandwidth requests from MACB.

2 GENERAL DESCRIPTION

Throughout this document, the term *MAC* refers to the *DQDB MACChip*.

The MAC implements the Queued Arbitrated functions of the Distributed Queue Dual Bus (DQDB) protocol according to the IEEE 802.6 (Metropolitan Area Network) standard. The chip supports STS3 rate at a nominal clock speed of 20MHz and was designed with 2.0 micron VLSI CMOS technology. It can also operate at DS3 rate at a nominal clock speed of 6MHz. Because a MAC is connected to only one bus, a typical DQDB node will have two MACs, one connected Bus A and another to Bus B.

The MAC performs three major tasks:

- Receiving cells that are addressed to this node

  When a new cell arrives, the Physical Layer signals the MAC by asserting the NewCell input coincident with the first byte of the cell. The Physical Layer then transmits data to the MAC at the rate of eight bits per clock cycle.

  The MAC monitors for cells with a Destination Address that matches its own address, or for cells with a Message Identifier that has been marked valid in the on-chip MID lookup table. If either condition is met, the MAC will copy the cell.

  To copy the cell, the MAC checks for errors, strips off cell header and trailer, and passes the payload in 32-bit words to the Reassembly unit of the Segmentation and Reassembly (SAR) board. In addition to data, the CellBegin, CellFull, CellValid, and CellEnd flags are transmitted to the Reassembly unit as status signals.

- Sending data to the Physical Layer

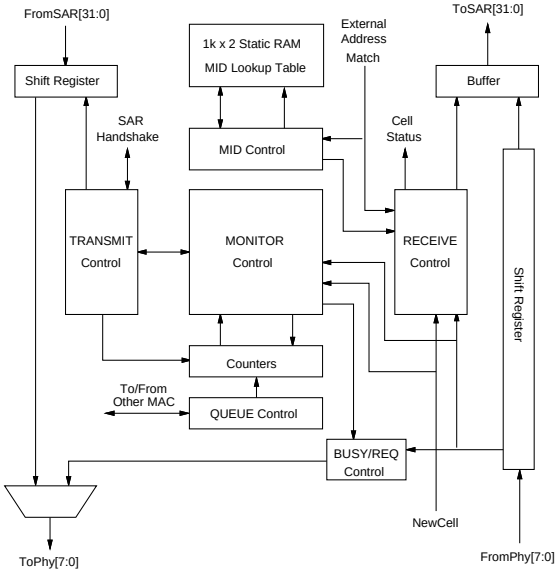
  When the node has data to send, the Segmentation unit (on the SAR board) asserts the SegSendReq signal. The MAC places the send request on it's DQDB queue.

  When the queueing counters indicate that sending is permitted, the MAC accepts 46 bytes of data from the Segmentation unit in 32-bit words, adds a header and trailer, and transmits the new cell via the Physical Layer at eight bits per clock cycle.

  Reception of the first word in each DQDB payload is acknowledged by assertion of the AckSeg signal to the Segmentation unit.

1 FEATURES:

- Implements Queued Arbitrated (QA) Functions of the Medium Access Control (MAC) sublayer protocol of the IEEE 802.6 standard (Metropolitan Area Network)
- Operates at STS-3 (155.520Mbps) and DS3 (44.736Mbps) rates
- Implements Bandwidth Balancing protocol
- Allows pre-loading of bandwidth balancing and timeout constants
- Provides on-chip MID lookup table
- Provides Scanning function
- 8-bit interface with Physical Layer
- 32-bit interface with the Segmentation and Reassembly board
- Provides TTL compatible I/O
- Requires a single 5V power supply

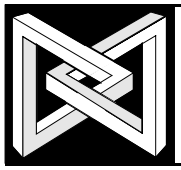


DQDB MAC Chip Data sh ee t

Frederick L. Burghardt Ting Y. Kao My T. Le

Abstract

This document describes an overview of The DQDB MAC Chip which implements the Distributed Queue Dual Bus protocol and operates at STS-3 or DS3 rate. The chip interfaces with 4 external units: the Segmentation and Reassembly Board, the Other MAC chip in the node, the Physical Layer, and the Host.



The
Bay
Bridge

Project Report: 10 Revision: 2.0
Department of Electrical Engineering
and Computer Sciences
University of California at Berkeley